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Application No. <u>09/695,516</u>	Prepared by <u>NB</u>	Tracking Number <u>05875719</u>	
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JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION	MESSAGE
a. Page Missing	<p>Please provide relationship of continuing data Serial nos. 09/603,023 and 09/608,317 in the continuing data paragraph (page 1 of specification).</p> <p>bib sheet shows = CONTINUATION (For both serial numbers)</p> <p>text reads = related.</p> <p>Please advise correct.</p> <p>Thank you</p> <p>initials <u>Trm</u></p>
b. Text Continuity	
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g. Brief Description	
h. Sequence Listing	
i. Appendix	
j. Amendments	
k. Other	
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Docket No.: TI-30674

HYBRID OF PREDICTIVE AND CLOSED-LOOP PHASE-DOMAIN DIGITAL PLL ARCHITECTURE

Related Patent Applications

5 This application claims the benefit, under 35 U.S.C. §119(e)(1), of U.S. Provisional Application No. 60/186,251, entitled *Hybrid of predictive/closed-loop digital PLL operation*, filed March 1, 2000 by Robert B. Staszewski and Dirk Leipold; and U.S. Provisional Application No. 60/198,907, entitled *PLL loop compensation scheme for the frequency/phase modulation*, filed April 20, 2000 by Robert B. Staszewski, Ken Maggio
10 and Dirk Leipold.

 This application is related to U.S. Patent Application S/N 09/603,023, entitled *Digital Phase-Domain PLL Frequency Synthesizer*, docket number TI-30677, filed June 26, 2000, by Robert B. Staszewski and Dirk Leipold; and U.S. Patent Application S/N 09/608,317, entitled *Digital Fractional Phase Detector*, docket number TI-30676, filed
15 June 30, 2000, by Robert B. Staszewski and Dirk Leipold, both applications assigned to the assignee of the present invention and incorporated by reference in their entirety herein.

Background of the Invention

20 1. Field of the Invention

 This invention relates generally to phase lock loops, and more particularly to an all-digital phase-domain phase-lock loop (PLL) that employs a hybrid of predictive and closed-loop architectures.

25 2. Description of the Prior Art

 Open-loop modulation techniques for data transmission are well-known in the prior art, and exhibit undesirable frequency wander and drift. Feed forward, closed-loop modulation techniques with phase-locked loop compensation for data transmission are also
30 well known in the prior art. These closed-loop solutions use an analog compensation that